ABSTRACT OF THE DISCLOSURE

Methods of forming capacitors, methods of forming capacitor-over-bit line memory circuitry, and related integrated circuitry constructions are described. In one embodiment, a capacitor storage node is formed having an uppermost surface and an overlying insulative material over the uppermost surface. Subsequently, a capacitor dielectric functioning region is formed discrete from the overlying insulative material operably proximate at least a portion of the capacitor storage node. A cell electrode layer is formed over the capacitor dielectric functioning region and the overlying insulative material. In another embodiment, a capacitor storage node is formed having an uppermost surface and a side surface joined therewith. A protective cap is formed over the uppermost surface and a capacitor dielectric layer is formed over the side surface and protective cap. A cell electrode layer is formed over the side surface of the capacitor storage node. In yet another embodiment, a plurality of capacitor storage nodes are formed arranged in columns. A common cell electrode layer is formed over the plurality of capacitor storage nodes. Cell electrode layer material is removed from between the columns and isolates individual cell electrodes over individual respective capacitor storage nodes. After the removing of the cell electrode layer material, conductive material is formed over portions of remaining cell electrode material thereby placing some of the individual cell electrodes into electrical communication with one another.